Partial translation of JP 2003-188495

[Claims]

[Claim 1]

A process for producing a printed wiring board comprising:
forming the first metal layer on one side or both sides of a polyimide film by a dry film forming method,
forming the second metal layer on the first metal layer by electroplating or electroless plating,
forming a pattern by a etching method, and
washing the etched surface with an oxidizer after etching.

[Claim 2]

The process for producing a printed wiring board according to Claim 1, wherein the first metal layer is formed from at least one selected from Ni, Cu, Mo, Ta, Ti, V, Cr, Fe, Co, and an alloy thereof.

[Claim 3]

The process for producing a printed wiring board according to Claim 1 or 2, wherein the oxidizer comprises at least one selected from potassium permanganate, potassium dichromate, and hydrogen peroxide.

[0036]

[Table 1]

	wiring pitch (μm)	retention time (hr)	insulation resistance (Ω)
Example 1	40	not less than 1000	1×10^{11}
Example 2	25	not less than 1000	1×10^{10}
Example 3	25	not less than 1000	1×10^{10}
Example 4	25	not less than 1000	4×10^{10}
Example 5	25	not less than 1000	2×10^{10}
Example 6	25	not less than 1000	8×10^{9}
Example 7	25	not less than 1000	1×10^{11}
Example 8	25	not less than 1000	1×10^{11}
Comparative Example 1	40	not less than 1000	1×10^{9}
Comparative Example 2	30	250	1×10^{4}
Comparative Example 3	40	not less than 1000	5×10^{9}
Comparative Example 4	30	300	1×10^{4}